WHAT IS CLAIMED IS:

1. A display comprising:

a plurality of stages of shift register circuits for sequentially driving a plurality of drain lines for supplying a video signal to pixels; and

a plurality of stages of first dummy shift register circuits arranged on the operation starting side of said plurality of stages of shift register circuits and not connected to said drain line;

wherein said shift register circuits and said first dummy shift register circuits include a first circuit section having a first transistor of first conductivity type connected to a first potential, a second transistor of first conductivity type connected to a second potential, and a third transistor of first conductivity type connected between the gate of said first transistor and said second potential for turning off said first transistor when said second transistor is in on state.

2. A display according to claim 1, further comprising a second dummy shift register circuit arranged on the side opposite to the operation starting side of said plurality of stages of shift register circuits and not connected to said drain line.

3. A display according to claim 1,

wherein a start signal is input to the first stage of said plurality of stages of first dummy shift register circuits.

4. A display according to claim 1,

wherein at least said first transistor, said second transistor and said third transistor are a p-type field effect transistor.

5. A display according to claim 1,

wherein a first capacitor is connected between the gate and the source of said first transistor.

6. A display according to claim 1,

wherein said third transistor has two gate electrodes electrically connected to each other.

7. A display according to claim 1,

wherein said first transistor is turned on in response to a clock signal.

8. A display according to claim 1, further comprising a diode-connected fourth transistor connected

between the gate of said first transistor and a clock signal line for supplying a clock signal.

9. A display according to claim 8,

wherein said diode-connected fourth transistor has two gate electrodes electrically connected to each other.

10. A display according to claim 1,

wherein said first circuit section further includes a fifth transistor of first conductivity type connected between the gate of said first transistor and a clock signal line for supplying a clock signal and operated to turn on in response to a signal turned on when said third transistor is in off state.

11. A display according to claim 1,

wherein said first circuit section includes a fourth transistor of first conductivity type connected to the gate of said first transistor and operated to turn on in response to a first signal, and a fifth transistor of first conductivity type connected between said fourth transistor and said first potential and operated to turn on in response to a second signal turned off when said first signal is in on state.

12. A display according to claim 11,

wherein a second capacitor is connected between the source of said first transistor and the junction point between said fourth transistor and said fifth transistor.

13. A display comprising:

a plurality of stages of shift register circuits for sequentially driving a plurality of drain lines for supplying a video signal to pixels; and

a dummy shift register circuits arranged on at least the side opposite to the operation starting side of said plurality of stages of shift register circuits and not connected to said drain line;

wherein said shift register circuits and said dummy shift register circuits include a first circuit section having a first transistor of first conductivity type connected to a first potential, a second transistor of first conductivity type connected to a second potential, and a third transistor of first conductivity type connected between the gate of said first transistor and said second potential for turning off said first transistor when said second transistor is in on state.

14. A display according to claim 13, further comprising two stages of dummy shift register circuits not

connected to said drain line and arranged on the operation starting side of said plurality of stages of shift register circuits.

15. A display according to claim 13,

wherein at least said first transistor, said second transistor and said third transistor are a p-type field effect transistor.

16. A display according to claim 13,

wherein a first capacitor is connected between the gate and the source of said first transistor.

17. A display according to claim 13,

wherein said third transistor has two gate electrodes electrically connected to each other.

18. A display according to claim 13,

wherein said first transistor is turned on in response to a clock signal.

19. A display according to claim 13, further comprising a diode-connected fourth transistor connected between the gate of said first transistor and a clock signal line for supplying a clock signal.

20. A display according to claim 19,

wherein said diode-connected fourth transistor has two gate electrodes electrically connected to each other.

21. A display according to claim 13,

wherein said first circuit section further includes a fifth transistor of first conductivity type connected between the gate of said first transistor and a clock signal line for supplying a clock signal and operated to turn on in response to a signal turned on when said third transistor is in off state.

22. A display according to claim 13,

wherein said first circuit section includes a fourth transistor of first conductivity type connected to the gate of said first transistor and operated to turn on in response to a first signal, and a fifth transistor of first conductivity type connected between said fourth transistor and said first potential and operated to turn on in response to a second signal turned off when said first signal is in on state.

23. A display according to claim 22,

wherein a second capacitor is connected between the

source of said first transistor and the junction point between said fourth transistor and said fifth transistor.